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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/771,465	02/05/2004	Hiroki Kanai	501.43494X00	2954

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EXAMINER	
BRADLEY, MATTHEW A.	

ART UNIT	PAPER NUMBER
2187	

DATE MAILED: 09/21/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/771,465	KANAI, HIROKI	
	Examiner	Art Unit	
	Matthew Bradley	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 June 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 29 June 2006 has been entered.

Claim Status

Claims 1-14 remain pending and are ready for examination.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims **1-14** are rejected under 35 U.S.C. 102(e) as being anticipated by Sanada et al (U.S. 6,484,245), hereinafter referred to as Sanada.

As per independents claim **1** and **8**, Sanada teach,

- a channel controller for receiving a file access input/output (I/O) request based on file-name indication from an information processing device

through a network, transmitting/receiving data to/from the information processing device and outputting a block access I/O request corresponding to the file access I/O request; (Figure 1 item 40 as taught in Column 4 line 58 to Column 5 line 8)

- a disk controller for carrying out input/output control of data stored in a storage volume for storing the data based on the block access I/O request output by said channel controller; (Figure 1 item 46 as taught in Column 5 lines 4-7)
- a first memory including a cache memory for temporarily storing the data delivered between the channel controller and the disk controller; and (Figure 1 item 45 as taught in Column 5 lines 2-3)
- a data transfer network connected to said channel controller, said disk controller and said first memory, (Figure 1 shown as the interconnections between items 44-46)
- wherein the channel controller is equipped with a first processor for outputting the block access I/O request corresponding to the file access I/O request and controlling the first memory, (Figure 1 item 44 as taught in Column 5 lines 1-8)
- a file access circuit which has a second processor and a second memory controlled by the second processor and serves to control the transmission/reception of the file access I/O request and the data sent

from the information processing device (Figure 1 item 42 'processor' and Figure 1 item 43 'memory' as taught in Column 4 lines 64-67),

- a data transfer device for controlling data transfer between the first memory and the second memory, (Column 6 lines 1-13)
- and a third memory controlled by the first processor, (Figure 1 item 47 as taught in Column 5 lines 1-8)
- which are formed on a circuit module, and, *The Examiner notes that as file servers are being taught by Sanada, it is inherent that the individual server components are formed on a circuit module.*
- wherein the second processor transmits information indicating the storage position of the data in the second memory to the first processor, (Column 5 lines 48-51)
- the first processor writes into the third memory data transfer information containing information indicating the storage position of the data in the first memory and information indicating the storage position of the data in the second memory, (Column 5 lines 1-8)
- and the data transfer device reads out the data transfer information from the third memory and controls the data transfer between the first memory and the second memory on the basis of the data transfer information thus read out (Column 5 lines 45-51).

As per independent claims **2** and **9**, Sanada teach,

- *The Examiner notes that independent claim 2 adds the following limitation to independent claim 1:*
  - transmits the storage position of the data transfer information in the third memory to the data transfer device, (Column 5 lines 5-8 and Column 5 lines 45-51)
- *The remaining limitations of claim 2 are rejected on the same grounds of rejection as independent claim 1.*

As per independent claims **3** and **10**, Sanada teach,

- *The Examiner notes that independent claim 3 adds the following limitation to independent claim 1:*
  - wherein the first processor writes into the third memory first data transfer information containing information indicating the storage position of the data in the first memory, (Column 5 lines 5-8)
  - the second processor writes into the second memory second data transfer information containing information indicating the storage position of the data in the second memory, (Column 5 lines 48-51)
  - and the data transfer device reads out the second data transfer information from the second memory, reads out the first data transfer information from the third memory, and controls the data transfer between the first memory and the second memory based on the first data transfer information and the second data transfer information (Column 5 lines 45-51).

The remaining limitations of claim 3 are rejected on the same grounds of rejection as independent claim 1.

As per independent claims **4** and **11**, Sanada teach,

- *The Examiner notes that independent claim 4 adds the following limitation to independent claim 1:*
  - and wherein the first processor writes into the third memory first data transfer information containing information indicating the storage position of the data in the first memory, the second processor writes into the second memory second data transfer information containing information indicating the storage position of the data in the second memory, (Column 5 lines 45-51)
  - the second processor transmits information indicating the storage position of the second data transfer information to the first processor, the first processor transmits to the data transfer device transfer start information containing information indicating the storage position of the first data transfer information and information indicating the storage position of the second data transfer information, (Use of item 47 Figure 1 as taught in Column 5 lines 45-51)
  - and the data transfer device reads out the second data transfer information from the second memory based on the transfer start information, reads out the first data transfer from the third memory on the basis of the transfer start information, and controls the data transfer

between the first memory and the second memory based on the first data transfer information and the second data transfer information (Column 5 lines 45-51).

The remaining limitations of claim 4 are rejected on the same grounds of rejection as independent claim 1.

As per dependent claims **5** and **12**, Sanada teach, wherein the data transfer device writes into the third memory information indicating the result of the data transfer carried out between the first memory and the second memory (Column 6 lines 11-13).

As per independent claims **6** and **13**, Sanada teach,

- a channel controller for receiving file access input/output (I/O) writing request based on a file-name indication, writing data from an information processing device through a network and outputting a block access I/O write request corresponding to the file access I/O writing request; (Figure 1 item 40 as taught in Column 4 line 58 to Column 5 line 8)
- a disk controller for writing the writing data into a storage volume in which data are stored based on the block access I/O write request; (Figure 1 item 46 as taught in Column 5 lines 4-7)
- a first memory including a cache memory for temporarily storing the writing data transmitted/received between the channel controller and the disk controller; and (Figure 1 item 45 as taught in Column 5 lines 2-3)

- a data transfer network connected to said channel controller, said disk controller and said first memory (Figure 1 shown as the interconnections between items 44-4)
- wherein the channel controller contains a first processor for outputting the block access I/O write request corresponding to the file access I/O writing request and controlling the first memory, (Figure 1 item 44 as taught in Column 5 lines 1-8)
- a file access circuit which has a second processor and a second memory controlled by the second processor and serves to receive the file access I/O writing request and the writing data from the information processing device, (Figure 1 item 42 'processor' and Figure 1 item 43 'memory' as taught in Column 4 lines 64-67)
- a data transfer device for controlling the data transfer between the first memory and the second memory, (Column 6 lines 1-13)
- and a third memory controlled by the first processor, (Figure 1 item 47 as taught in Column 5 lines 1-8)
- which are formed on a circuit module, and *The Examiner notes that as file servers are being taught by Sanada it is inherent that the individual server components are formed on a circuit board.*
- wherein the first processor writes into the third memory first data transfer information containing information indicating the storage position of the writing data in the first memory, the second processor writes into the second memory second data transfer information containing information indicating the storage

position of the writing data in the second memory and transmits information indicating the storage position of the second data transfer information to the first processor, (Column 5 lines 1-8)

- the first processor transmits the data transfer device transfer start information containing information indicating the storage position of the first data transfer information and information indicating the storage position of the second data transfer information, the data transfer device reads out the second data transfer information from the second memory based on the transfer start information, reads out the first data transfer information from the third memory based on the transfer start information and transfers the writing data from the second memory to the first memory based on the first data transfer information and the second data transfer information, (Column 5 lines 1-8 and Column 6 lines 1-13)
- and the disk controller writes into the storage volume the writing data stored in the first memory on the basis of the write request (Column 6 lines 1-13).

As per independent claims **7** and **14**, Sanada teach,

- a channel controller for receiving a file access input/output (I/O) read- out request based on a file-name indication from an information processing device through a network, transmitting to the information processing device read-out data read out from a storage volume for storing data and outputting a block access I/O read request corresponding to the file access I/O read-out request; (Figure 1 item 40 as taught in Column 4 line 58 to Column 5 line 8)

- a disk controller for reading out the read-out data from the storage volume based on the block access I/O read request; (Figure 1 item 46 as taught in Column 5 lines 4-7)
- a first memory including a cache memory for temporarily storing the read-out data transmitted/ received for the storage volume between the channel controller and the disk controller; and (Figure 1 item 45 as taught in Column 5 lines 2-3)
- a data transfer network connected to said channel controller, said disk controller and said first memory (Figure 1 shown as the interconnections between items 44-46)
- wherein the channel controller comprises a first processor for outputting the block access I/O read request corresponding to the file access I/O read-out request and controlling the first memory, (Figure 1 item 44 as taught in Column 5 lines 1-8)
- a file access circuit which has a second processor and a second memory for controlling the second processor and receives the file access I/O read-out request from the information processing device, (Figure 1 item 42 'processor' and Figure 1 item 43 'memory' as taught in Column 4 lines 64-67)
- a data transfer device for controlling the data transfer between the first memory and the second memory, and (Column 6 lines 1-13)
- a third memory controlled by the first memory, (Figure 1 item 47 as taught in Column 5 lines 1-8)

- which are formed on a circuit board, *The Examiner notes that as file servers are being taught by Sanada, it is inherent that the individual server components are formed on a circuit board.*
- and wherein the disk controller writes into the first memory the read-out data read out from the storage volume based on the read request, the first processor writes into the third memory first data transfer information containing information indicating the storage position of the read-out data in the first memory, the second processor writes into the second memory second data transfer information containing information indicating the storage position of the read-out data in the second memory and transmits information indicating the storage position of the second data transfer information to the first processor, (Column 5 lines 1-8)
- transmits to the data transfer device transfer start information containing information indicating the storage position of the first data transfer information and information indicating the storage position of the second data transfer information, the data transfer device reads out the second data transfer information from the second memory based on the transfer start information, reads out the first data transfer information from the third memory based on the transfer start information and transfers the read-out data from the first memory to the second memory on the basis of the first data transfer information and the second data transfer information , and the second

processor transmits the read-out data stored in the second memory to the information processing device. (Column 5 lines 45-51).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew Bradley whose telephone number is (571) 272-8575. The examiner can normally be reached on 6:30-3:00 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald A. Sparks can be reached on (571) 272-4201. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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